A Low-Noise Baseband 5-GHz Direct-Coupled HBT Amplifier with Common-Base Active Input Match

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***Abstract*—This paper reports on an HBT direct-coupled 2-stage amplifier that uses active common-base input matching to provide multi-decade frequency performance from dc to 5 GHz. This work benchmarks the first reported HBT noise results of an HBT amplifier using common-base active input matching. The 2-stage amplifier consists of a common-base input stage that is directly coupled to a Darlington feedback amplifier output stage. The common-base input can be bias tuned to achieve >13-dB return loss at 3 GHz and a minimum noise figure of 2.9 dB at 1 GHz. A gain of 17.5 dB with a 3-dB bandwidth greater than 5 GHz was achieved under low-noise input bias. This amplifier topology can be implemented without the use of a complex microwave process, which typically integrates backside vias and microstrip matching components. The compact amplifier consumes an area of 0.82 × 0.47 mm^2, which is 10 times smaller than a previously reported 2.5–4 GHz narrow-band passive matched HBT amplifier with similar noise and gain performance.**

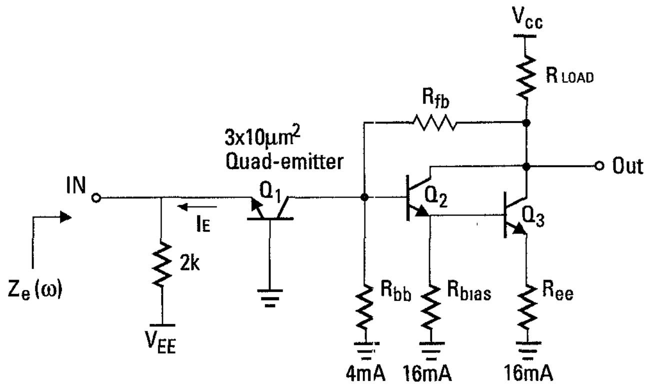

Fig. 1. Detailed schematic of the 2-stage direct coupled HBT amplifier with common-base active input match stage.

I. Introduction

Active techniques are commonly used in FET technology in order to economically realize broadband impedance matching and balun networks in a small chip area. A technique that is utilized in MESFET to achieve broadband input matching is the common-gate input stage configuration [1]–[3]. This technique has the advantage of being able to match the input to 50 ohms, as well as for low noise figure, without the use of large, passive microstrip-matching networks. A common-gate configuration also lends itself to broadband impedance and gain performance due to the absence of miller capacitance multiplication at the input that is present in common-source topologies. Using this technique, broadband impedance matching from dc to microwave frequencies is achievable. This is attractive for applications such as test instrumentation, light-wave fiber optic communication, digital IC's, and modulator-demodulator IC's.

The Heterojunction Bipolar Transistor (HBT) is attractive for these applications because of its high-speed microwave digital capabilities and superior analog characteristics, such as its high device transconductance and good dc beta and threshold-matching properties. A wideband low cost direct-coupled HBT amplifier would have generic use in these applications. One popular direct-coupled bipolar design is the Darlington feedback amplifier. This amplifier is capable of dc to >10 GHz frequency performance using AlGaAs-GaAs HBT's [4]–[7]. However, the feedback nature of the design lends itself to high noise figures of ≈5–6.5 dB [4].

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By implementing a common-base input stage with the Darlington feedback amplifier, a minimum noise figure of 2.9 dB was obtained while maintaining the multi-decade gain-bandwidth performance of the Darlington amplifier stage. The resulting active matched amplifier chip is 10 times smaller than a previously reported 2.5–4 GHz passive matched HBT amplifier, which was 2.5×1.65 mm^2 in size, and obtained a minimum noise figure of 3.7 dB and an associated gain of 15 dB at 3 GHz [8]. The following sections will describe the active matched amplifier design and measured results.

II. Common-Base Direct-Coupled Amplifier

The HBT direct-coupled amplifier consists of a common-base stage that is directly coupled to a Darlington feedback amplifier stage, shown in Fig. 1. The Darlington stage is almost identical to the design previously reported in [4]. The Darlington amplifier consists of transistor pair Q_2 and Q_3, parallel and series feedback resistors R_{fb} and R_{ee}, biasing resistors R_{bias} and R_{bb}, and load resistor R_{load}. Transistors Q_2 and Q_3 are 2×10 μm^2 four-finger HBT's biased at ≈16 mA each, and a V_{ce} equal to 2.6 and 4.0 V, respectively. The Darlington stage is self-biased through a 12-V supply voltage (V_{cc}). The active matched input stage consists of a common-base transistor, Q_1, which is grounded at its base to extend its frequency operation down to dc. Transistor Q_1 is a 3×10 μm^2 quad-emitter HBT chosen for its low emitter resistance and good noise figure performance. Resistor R_{2k} is an emitter bias resistor that is connected to a negative supply voltage, $V_{ee} \approx -2.3$ V. This bias voltage sets the common-base emitter bias current I_e. This bias current can be tuned for optimum noise figure or input return-loss performance.

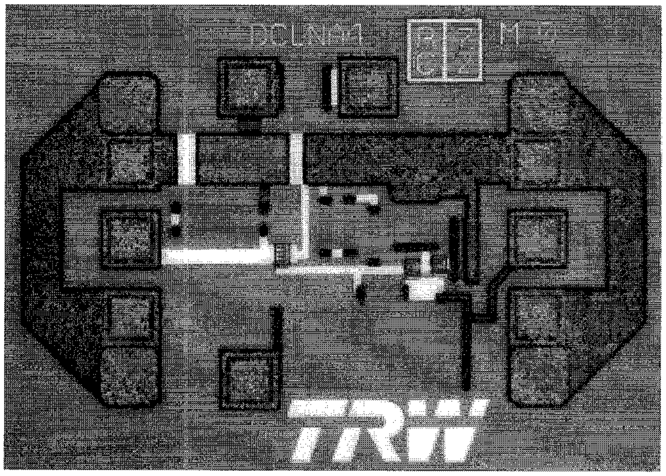

Fig. 2. Micro-photograph of the fabricated chip. The chip size is 0.82×0.47 mm^2.

The input return-loss of the common-base stage is determined by the input impedance looking into the emitter of the common-base transistor Q_1. This is given by the following expression:

$$Z_e(\omega) = r_e + \frac{nKT}{qI_c} + \frac{r_b}{1 + \frac{\beta_0}{\sqrt{1+\omega^2 \cdot r_\pi^2 \cdot c_\pi^2}}} \tag{1}$$

where r_e, r_b, and r_π are the HBT hybrid-π model resistance parameters, C_π is the input shunt capacitance, β_0 is the low frequency ac current gain, $I_c \approx I_e$ is the bias current, n is the ideality factor, T is the temperature in Kelvin, and q and K are physical constants. From this expression, it is obvious that the input impedance is strongly dependent on bias current I_e. The last term in (1) shows the frequency dependence of the input impedance.

The input return-loss is then defined by the following expression:

$$\mathrm{RL} = 20 \cdot \mathrm{LOG}\left[\frac{Z_0 - Z_e(\omega)}{Z_0 + Z_e(\omega)}\right] \tag{2}$$

where Z_0 is the system impedance (50 Ω) and RL is measured in dB.

For a 3×10 μm^2 quad-emitter HBT (Q_1): if $r_e \approx$1.3 Ω, $r_b \approx$8.5 Ω, β_0 =60, and $1/(2\pi R_\pi C_\pi)$ =330 MHz, then in order to achieve an input impedance of 50 Ω at low frequencies ($Z_e(0) \approx$50 Ω), the common-base stage must be biased at 0.63 mA. This bias condition corresponds to an input return-loss >15 dB. Test data, however, shows that this bias condition does not correspond to optimum noise figure performance of the common-base transistor.

III. Measured Results

Fig. 2 shows a photograph of the fabricated direct-coupled amplifier chip that is 0.82×0.47 mm^2 in area. The conventional Darlington amplifier reported in [4] was 0.5×0.7 mm^2 in area. Much of the area of these chips, however, is consumed by a coplanar ground strip and rf probe pads. An optimized production chip could fit in an area of 0.35×0.35 mm^2 including the active match stage.

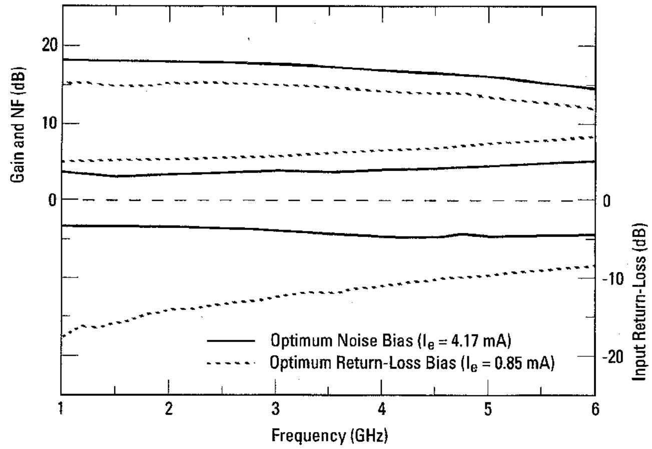

Fig. 3. Broadband gain, noise figure, and return-loss performance at optimum noise and return-loss bias.

Fig. 3 gives the gain, noise figure, and input return-loss at optimum return-loss and noise figure bias conditions. Under optimum noise bias (I_e =4.17 mA), the gain is 17.5 dB with a 3-dB bandwidth of greater than 5 GHz and a noise figure range from 2.9–4.8 dB over the 1–6 GHz frequency range. Below 1 GHz, the gain has a flat response down to dc while the noise figure is flat down to the $1/f$ corner frequency of the HBT devices. The measured $1/f$ HBT corner frequencies can range from 1–100 kHz. Below this frequency, the noise figure of the amplifier is predicted to increase inversely with frequency. The input return-loss under this low noise bias condition is only 3.8 dB. Under optimum input return-loss bias (I_e =0.85 mA) the return-loss is 17 dB at 1 GHz and degrades to 8 dB at 6 GHz. The corresponding gain is 13.8 dB with a bandwidth greater than 5 GHz, and a noise figure that ranges from 5–7.9 dB across the 1–6 GHz band.

Fig. 4 gives the gain, input return-loss, and noise figure at 3 GHz versus the common-base emitter bias current, I_e. This figure illustrates the trade-off between optimum return-loss and noise bias. As I_e is reduced from 4.17 mA to 0.85 mA, approaching the optimum return-loss bias of I_e =0.63 mA, the input return-loss improves from -3.8 to -11.6 dB. Correspondingly, the noise figure increases from 3.7 to 5.74 dB, while the gain drops from 17.5 to 13.8 dB. At higher I_e, the return-loss is poorly matched to 50 Ω, however the device g_m increases, which improves the gain and noise figure match. Fig. 4 also shows the input return-loss predicted from (1) and (2), the dotted line, which is plotted against the measured return-loss over bias current, I_e. Equations (1) and (2) predict the return-loss to within 1 dB over most of the bias range.

IV. Conclusion

An HBT 2-stage direct-coupled amplifier with common-base active input match was demonstrated. By directly coupling a common-base stage to the input of a Darlington amplifier, the noise figure of the Darlington was improved by 1.5–3.0 dB while maintaining wide gain-bandwidth performance. The resulting 2-stage amplifier achieved 17.5 dB gain to 5 GHz with a minimum noise figure of 2.9 dB under low noise bias. The common-base active match was implemented

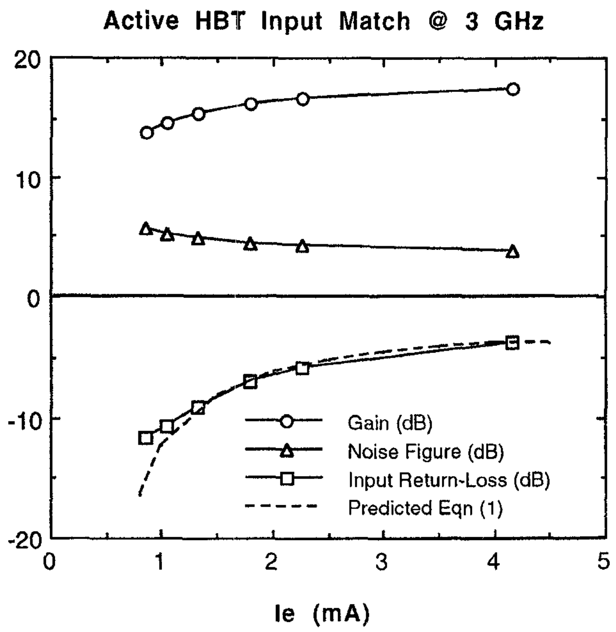

Fig. 4. Gain, return-loss, and noise figure at 3 GHz versus common-base emitter current bias, I_e.

with little impact on size. The resulting chip is 10 times smaller than a previously reported passive matched HBT amplifier with similar performance. In combination with a low cost HBT production technology, this active matching technique can be useful for many commercial applications that require baseband (kHz) to microwave frequency performance.

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